Research and Development Section
Indian Institute of Technology Guwahati
Guwahati-781039, Assam

Applications are invited for an **Online** and **Offline Walk in interview** for the following post(s) in the project entitled, **" Design and Development of AI/ML Co-Processor and Post Quantum Cryptography Co-Processor (An initiative towards Electronics System Design and Manufacturing in North-East Region)"** at the department of Electronics and Electrical Engineering, IIT Guwahati.

Project Duration: 03 Years
Date: 08 September 2023 (Friday) (NOTE: In case interviews are not finished on 08 September, it will continue on 09 and 10 September 2023. Therefore, please make yourself available from 08 September – 10 September 2023)
Time: 10.00 AM – 1.00 PM and **2.00 PM – 5.00 PM**

Venue: EEE Conference Room or **EEE Meeting Room** in the main academic complex for the in-person interviews. **WebEx/Google Meet link** will be sent by email to the shortlisted candidates for the online interviews.

Sl. No.	Project Staff Designation	Number of Vacancies	Pay (Rs.)	HRA (Rs.)	Medical (Rs.)	Total (Rs.)	Duration in months	Qualifications
1	**Principal Scientist**	2	125000	22500	1250	148750	06	(1) Ph. D in EC/EE/CS with 3 years of relevant experience or (2) MTech/ME in VLSI/ Microelectronics/ CS with 6 Years of relevant experience or (3) BTech/BE in EC/EE/CS with 8 years' relevant experience. Candidates having the knowledge of chip signoff/tape-out and the commercial EDA tools and the VLSI Design flow are preferred.
2	**Senior Project Engineer**	2	75000	13500	1250	89750	06	(1) Ph. D in EC/EE/CS or (2) MTech/ME in VLSI/ Microelectronics/CS with 4 Years of relevant experience or (3) BTech/BE in EC/EE/CS with 6 years relevant experience. Candidates having the knowledge of chip signoff/tape-out and the commercial EDA tools and the VLSI Design flow are preferred.

3	**Senior Project Engineer**	1	75000	13500	1250	89750	06	(1) Ph. D in EC/EE/CS or (2) MTech/ME in VLSI/ Microelectronics/CS with 4 Years of relevant experience or (3) BTech/BE in EC/EE/CS with 6 years' relevant experience. Candidates having the knowledge of chip signoff/ tape-out and the commercial EDA tools and the VLSI Design flow are preferred. Note that the selected candidate would be posted at **Bangalore** to execute VLSI chip design, signoff/ tape-out work of the project. It is desired to have following qualifications in the person being posted at **Bangalore**. HE/SHE should be the coordinator and the contact between the chip production plants and designers as a chip manufacturing support engineer. HE/SHE will undergo an intensive training, and will be in charge of the full tape out of the chips designed by designers. HE/SHE would in charge of the following tasks during the tape out process: (A) Check and guarantee the quality of designed chips. (B) Prepare the chip design for foundry manufacturing and assist the designer with final sign-off. You accomplish this with the help of advanced EDA tools. (C) Hold technical discussions with designer to lead them through the sign-off process. (D) Assist the designer in obtaining the necessary foundry information and documentation before to, during, and after chip design and fabrication. (E) Monitor projects from conception to finish and ensure that all project milestones are met. (F) Hold technical discussions with the manufacturing plants that make these chips.
4	**Project Scientist-1**	14	56000	10080	1250	67330	06	PhD in VLSI/ Microelectronics/ CS, or MTech/ME in VLSI/ Microelectronics/ CS with 2 Years of relevant experience or (2) BTech/BE in EC/EE/CS with 4 years' relevant experience. Candidates having the knowledge of chip signoff/tape-out and the commercial EDA tools and the VLSI Design flow are preferred.

5	**Project Scientist-1**	1	56000	10080	1250	67330	06	PhD in VLSI/ Microelectronics/ CS, or MTech/ME in VLSI/ Microelectronics/CS with 2 Years of relevant experience or (2) BTech/BE in EC/EE/CS with 4 years' relevant experience. Candidates having the knowledge of chip signoff/tape-out and the commercial EDA tools and the VLSI Design flow are preferred. Note that the selected candidate would be posted **at New Delhi (NCR)** to facilitate the project activities. It is desired to have the candidate having responsible for administering and project management including monitoring and reviewing technical and financial activities under the project with following know-how. Understand of hardware design (ASIC/FPGA), knowledge of HDLs like Verilog/ System Verilog, working knowledge of ASIC design flow, design expertise spanning all phases of the VLSI design cycle and the knowledge about various EDA tools & Licensing Policies are expected in the candidate. HE /SHE should have team management / team leading capabilities. Knowledge of project management tools is desirable along with interpersonal and excellent project management skills, good communication skills, client interaction capability and the quick grasping of technical scopes.

Note-1: It is to be noted that the project duration is of 03 years and the appointments will be continued/renewed till 03 years from the date of the appointment or the completion of the project whichever is earlier, based on the performance.

Application Process: Interested candidates may apply for the online/in-person interview at the links given below for the corresponding positions giving details of all educational qualifications, experience, contact address, phone no., email etc.

Principal Scientist: https://forms.gle/PGc5AwFm7qjraGhG8
Senior Project Engineer: https://forms.gle/53mu225BAfjc4ZVWA
Project Scientist-1: https://forms.gle/SaMYjM8WWPLSy9VeA

Candidates need to upload the relevant documents in the PDF format only at the registration links given above by **05 September 2023 (Tuesday**) till **05.00 PM**. Candidates will be shortlisted based on the qualifications posted in the advertisement and, later only shortlisted candidates will be intimated by email separately to attend interviews.

Note-2: In case of large number of applications received for various posts, an online written test having questions on mental or quantitative/qualitative abilities may be conducted on **07 September 2023**. The duration of this written test, if conducted, will be of **ONE Hr.** having **maximum 100 questions** with negative marking. It is to be further noted that candidates may be shortlisted for final interview based on the qualifications posted in the advertisement and the performance in the written test both, in case a written test is conducted because of large number of applications received for various positions advertised. It is the responsibility of the candidates attending online interviews to have a very good and stable network connectivity.

Last date for applying for the above-mentioned positions is 05 September 2023.

Selection Process: The shortlisted candidates have to appear in the online or in-person interview. A choice must be filled during the online form submission. Selection will be based on the performance of the candidate in the interview. The selection committee will decide the suitable candidate after the interview. Candidates will not be sent any call letter separately.

For any clarification, contact: Dr. Gaurav Trivedi (Principal Investigator)
Email: trivedi@iitg.ac.in
Phone: +91-361-2583199 (**Preferred contact time is from 10.00AM – 5.00PM**)

No campus accommodation will be available for the selected candidates.
No TA/DA will be paid to the candidates for appearing in the test and interview.

EEESPNMEIT00883xxGT008-ZBSA-2354 **Assistant Registrar (R&D)**